WHAT IS CLAIMED IS:

1. An image data compensation method to convert image data, indicating gray levels of pixels aligned in a matrix in an X direction and a Y direction, into analog data and to compensate the image data when a voltage signal is supplied to each of the pixels, a polarity of the voltage signal being inverted based on a predetermined constant potential every predetermined period, comprising the steps of:

storing reference compensation data corresponding to specific levels among levels available to the image data for each pair of reference coordinates preset in a display region in which the pixels are aligned;

interpolating the stored reference compensation data in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates and storing the first compensation data in association with the each pair of reference coordinates and the levels;

selectively reading, from the stored first compensation data, pieces of data which correspond to pairs of reference coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of the image data;

interpolating the read first compensation data in the coordinate directions to generate second compensation data which corresponds to the image data; and

adding the second compensation data to the image data in at least one of a case in which the voltage signal is positive, and a case in which the voltage signal is negative with respect to the constant potential, whereby the image data is compensated.

2. An image data compensation circuit that converts image data, indicating gray levels of pixels aligned in a matrix in an X direction and a Y direction, into analog data and that compensates the image data when a voltage signal is supplied to each of the pixels, a polarity of the voltage signal being inverted based on a predetermined constant potential every predetermined period, comprising:

a memory that stores reference compensation data corresponding to specific levels among levels available to the image data for each pair of reference coordinates preset in a display region in which the pixels are aligned;

an interpolation processor that interpolates the reference compensation data stored in the memory in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates;

a compensation table that stores the first compensation data in association with the reference coordinates and the levels;

a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspond to pairs of reference coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of the image data;

an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data; and

an adder that adds the second compensation data to the image data in at least one of a case in which the voltage signal is positive and a case in which the voltage signal is negative with respect to the constant potential, whereby the image data is compensated.

3. The image data compensation circuit according to Claim 2, the adder adding the second compensation data to the image data in only one of the case in which the voltage signal is positive and the case in which the voltage signal is negative; and in the other one of the case in which the voltage signal is positive and the case in which the voltage signal is negative, the adder adding a substantially zero value to the image data.

4. The image data compensation circuit according to Claim 3, the reference compensation data corresponding to the specific level being a value adjusted so as to reduce the difference in the gray level between the one case in which the sum of the reference compensation data and the image data corresponding to the specific level is applied to a pixel electrode and the other case in which the reference compensation data is not added to the image data corresponding to the specific level and the image data is applied to the pixel electrode.

5. The image data compensation circuit according to Claim 2, the reading unit including:

an X counter that counts first clock signals which are used as a time reference for X-direction scanning in the display region and that generates X-coordinate data indicating the X coordinate of the pixel corresponding to the image data in the display region;

a Y counter that counts second clock signals which are used as a time reference for Y-direction scanning in the display region and for generating Y-coordinate data indicating the Y coordinate of the pixel corresponding to the image data in the display region; and

an address generator that specifies a plurality of pairs of reference coordinates positioned near the coordinates of the pixel corresponding to the image data based on the X-coordinate data and the Y-coordinate data and that generates addresses to read the corresponding first compensation data from the compensation table based on the specified pairs of reference coordinates and the level of the image data,

the arithmetic unit performing interpolation in accordance with the distance from the coordinates of the image data specified by the X-coordinate data and the Y-coordinate data to each of the specified pairs of reference coordinates corresponding to the read first compensation data.

6. The image data compensation circuit according to Claim 5, the memory, the interpolation processor, the X counter, and the Y counter being shared among RGB colors, and the compensation table, the arithmetic unit, the address generator, and the adder being provided in association with each of the RGB colors.

7. The image data compensation circuit according to Claim 2, the pixel including a liquid crystal capacitor formed of two electrodes and liquid crystal provided therebetween, and

the specific levels to which the reference compensation data correspond including first and second levels corresponding to first and second points at which a display characteristic curve indicating at least one of transmissivity and reflectivity with respect to the effective value of a voltage applied to the liquid crystal capacitor suddenly changes and at least one level between the first and second levels.

8. The image data compensation circuit according to Claim 7,

the interpolation processor operating so as to:

interpolate the reference compensation data to generate the first compensation data corresponding to levels ranging from the first level to the second level,

use the reference compensation data corresponding to the first level for the first compensation data corresponding to levels below the first level, and

use the reference compensation data corresponding to the second level for the first compensation data corresponding to levels exceeding the second level;

the compensation table operating so as to:

store the first compensation data for levels ranging from the first level to the second level; and

the reading unit operating so as to:

select data corresponding to the first level from the first compensation data stored in the compensation table when the level of the image data is below the first level,

select data which is generated in accordance with the level of the image data when the level of the image data is within a range between the first level and the second level, and

select data corresponding to the second level when the level of the image data exceeds the second level.

9. The image data compensation circuit according to Claim 8, further comprising:

a coefficient output unit that outputs a coefficient in accordance with the difference between the level of the image data and the first or second level when the level of the image data is below the first level or exceeds the second level; and

a multiplier that multiplies the read first compensation data corresponding to the first or second level by the coefficient output from the coefficient output unit,

the arithmetic unit performing interpolation according to the coordinates by using the product obtained by the multiplier as the first compensation data which is selectively read by the reading unit.

10. The image data compensation circuit according to Claim 9, the coefficient output unit including:

a look up table that stores coefficients corresponding to at least two levels in a region in which the level of the image data is below the first level or in a region in which the level of the image data exceeds the second level; and

a coefficient interpolating unit that interpolates the coefficients stored in the look up table and computing a coefficient corresponding to the image data.

11. The image data compensation circuit according to Claim 5,

the image data and the reference compensation data corresponding to each of the RGB colors,

the interpolation processor generating the first compensation data in association with each of the RGB colors, and

the compensation table, the arithmetic unit, and the adder being provided in association with each of the RGB colors.

12. The image data compensation circuit according to Claim 11, the amount of reference compensation data for G being larger than that for R or for B.

13. The image data compensation circuit according to Claim 12, the reference coordinates corresponding to the reference compensation data for R or B being extracted from the reference coordinates corresponding to the reference compensation data for G based on specific rules.

14. An image data compensation circuit that converts image data, indicating gray levels of pixels aligned in a matrix in an X direction and a Y direction, into analog data and that compensates the image data when a voltage signal is supplied to each of the pixels, a polarity of the voltage signal being inverted based on a predetermined constant potential every predetermined period, comprising:

a memory that stores white reference compensation data which corresponds to a white reference level, black reference compensation data which corresponds to a black reference level, and at least one piece of intermediate reference compensation data which corresponds to a level between the white reference level and the black reference level;

a first compensation data generator that interpolates the pieces of reference compensation data in the memory in the level directions based on half tone image data of the image data in one polarity and for generating first compensation data;

a second compensation data generator that interpolates coordinate data for the half tone image data and the first compensation data in the coordinate directions and for generating second compensation data; and

an adder that adds the second compensation data to the half tone image data, whereby the half tone image data is compensated.

15. The image data compensation circuit according to Claim 14, when the image data in the one polarity is at the white or black reference level, the first compensation data generator using the white reference compensation data or the black reference compensation data in the memory as the first compensation data.

16. The image data compensation circuit according to Claim 14, when the image data in the one polarity is at the white or black reference level, the first compensation data generator using the product of the white reference compensation data or the black reference compensation data in the memory and a coefficient in accordance with the difference between the image data at the white or black reference level and the white reference compensation data or the black reference compensation data in the memory as the first compensation data.

17. The image data compensation circuit according to Claim 14, the intermediate reference compensation data in the memory being computed based on a deficiency or an

excess of luminance level in positive polarity and negative polarity in a region generated by dividing a screen.

18. A liquid crystal display, comprising;

a memory that stores reference compensation data corresponding to specific levels among levels available to image data, indicating the gray levels of pixels aligned in the form of a matrix in the X direction and the Y direction, for each pair of reference coordinates preset in a display region in which the pixels are aligned;

an interpolation processor that interpolates the reference compensation data stored in the memory in the level directions and that generates first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates;

a compensation table that stores the first compensation data in association with the reference coordinates and the levels;

a reading unit that selectively reads, from the first compensation data stored in the compensation table, pieces of data which correspond to pairs of reference coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of the image data;

an arithmetic unit that interpolates the read first compensation data in the coordinate directions and that generates second compensation data corresponding to the image data;

an adder that adds the second compensation data to the image data at least in one of a case in which a voltage signal is positive and a case in which the voltage signal is negative with respect to a predetermined potential, whereby the image data is compensated;

a D/A converter that converts the compensated image data into analog data;

a polarity inverter circuit that inverts the polarity of the voltage signal on the basis of the predetermined potential every predetermined period; and

a driving circuit that supplies the inverted voltage signal to each of the pixels.

19. An electronic apparatus, comprising:

the liquid crystal display as set forth in Claim 18.